NATIONAL DEVELOPMENT PLAN 2020

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Final results of the ERDF project No. 1.1.1.1/16/A/203 "Multilayer silicon nanocapacitor with improved dielectric layers"

After the midterm of the project (28 Feb 2018) and until the end of its implementation, the work focused on testing the repeatability of the manufacturing technology of a nanocapacitor with a multilayer Si_3N_4 dielectric, as well as developing a prototype of the corresponding manufacturing technology in a laboratory environment. The implementation of the project was completed on February 29, 2020.

As a result of the project, a method for depositing a multilayer Si_3N_4 dielectric for applications in nanocapacitors was developed. According to this method, several Si_3N_4 nanolayers are deposited on top of each other using a chemical vapour deposition method in a chemical reaction between the gases silane (SiH_4) and ammonia (NH_3): $3SiH_4 + 4NH_3 \rightarrow Si_3N_4 + 12H_2$. After deposition of each nanolayer, the supply of SiH_4 gas to the deposition reactor is stopped and the surface of the deposited Si_3N_4 is annealed at 700-800 ºC in the NH_3 gas stream. After annealing, the SiH_4 gas supply is resumed again and the next Si_3N_4 nanolayer is deposited. Deposition of the nanolayers and annealing of their surface in the NH_3 gas stream is repeated until the desired number of dielectric Si_3N_4 nanolayers is reached.

The developed method of dielectric deposition prevents the formation of pinhole defects in a thin dielectric layer. Pinholes are a typical type of defect in thin dielectric layers, the probability of which increases with a decrease in the thickness of the dielectric layer to several nanometers. Pinhole defects can cause an electrical short circuit between the top and bottom electrodes of the capacitor, and pinhole defects reduce the breakdown voltage of the capacitor. Pinhole defects can be prevented by fabricating a dielectric from several nanolayers of the same material superimposed on each other. In this case, each subsequent layer covers the pinhole defects of the previous layer, as shown schematically in Figure 1.

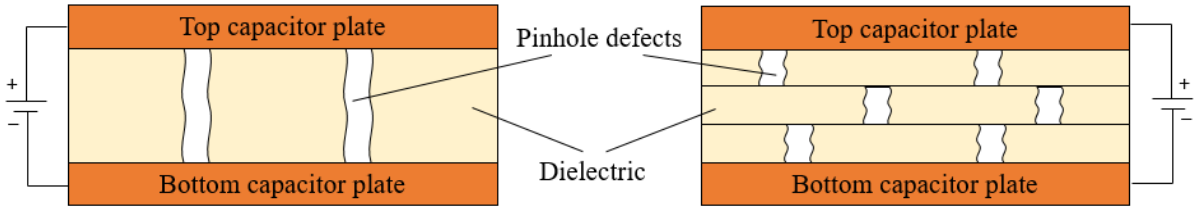

Fig. 1. Prevention of the pinhole defects in a multilayer dielectric: on the left – a single-layered dielectric in which pinhole defects grow through the full thickness of the dielectric; on the right – a multilayer dielectric in which each subsequent dielectric nanolayer covers the pinholes of the previous nanolayer.

On December 23, 2019, we submitted ***a patent application*** No. P-19-17 " Deposition method of a thin multilayer dielectric" to the Latvian Patent Office (LPO). Publication A of the patent application (LV15492A) was published in the Official Gazette of LPO on March 20, 2020 (page 305): https://www.lrpv.gov.lv/sites/default/files/20200320.pdf#page=305

Based on the developed method of multilayer Si_3N_4 dielectric deposition, the project resulted in the development of two prototypes of the nanocapacitor fabrication technology. The thickness of the multi-layered Si_3N_4 dielectric in the developed prototypes was 40 and 60 nm (Table 1). ***The first prototype*** (Figure 2) is a nanocapacitor with the bottom electrode made from polycrystalline silicon (Poly-Si). Polycrystalline silicon is a typical material used for manufacturing electrodes in microelectronic components. The mid-term results of the project showed that the Poly-Si electrode has a grainy structure and its surface roughness is comparable to the thickness of the Si_3N_4 nanolayer when the Si_3N_4 nanolayer is a few tens of nanometers thick[1]. In this case, the roughness of the Si_3N_4 nanolayer replicates the roughness of Poly-Si. Increased roughness of the dielectric is undesirable in the case of a nanocapacitor because this increases the leakage current and the probability of dielectric breakdown.

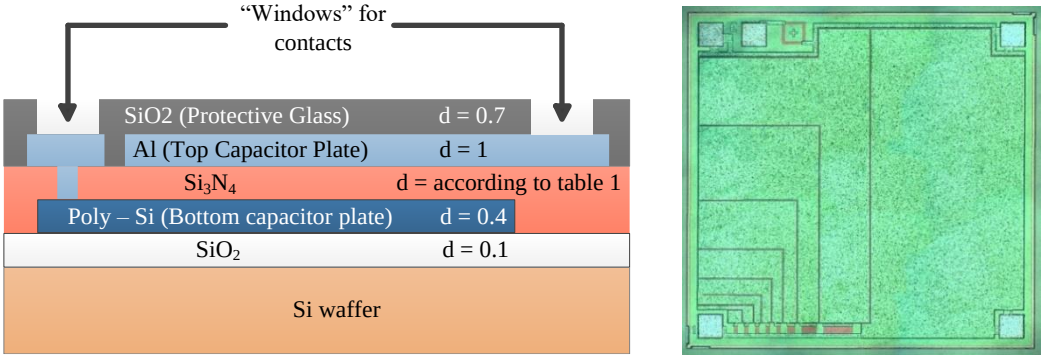

Fig. 2. Prototype 1 is a nanocapacitor that has a bottom electrode made from Poly-Si. The structure of the layers is shown on the left-hand side. The capacitor topology is shown on the right-hand side. The area of one capacitor area is 2.95 mm^2, *d* is the thickness of the layers (in μm). The parameters of the Si_3N_4 dielectric are shown in Table 1.

To eliminate the drawback of the Poly-Si electrode, we developed ***the second prototype*** of the nanocapacitor fabrication technology (Figure 3). This prototype uses a low-resistivity Si wafer as a bottom electrode of the nanocapacitor. The roughness of the Si wafer is only about 0.1 nm, which does not influence the roughness of Si_3N_4 nanolayer deposited on the top of it[1].

Table 1

Parameters of the multi-layered Si_3N_4 dielectric – thickness and number of nanolayers

Thickness (*d*) of the multi-layered Si_3N_4 dielectric, nm	Number of Si_3N_4 nanolayers in the dielectric
40	5
60	5

[1] Avotina, L., Pajuste, E., Romanova, M., Enichek, G., Zaslavskis, A., Kinerte, V., Avotins, J., Dekhtyar, Yu., Kizane, G. Surface morphology of single and multilayer silicon nitride dielectric nano-coatings. *Materials Science (Medžiagotyra)*, 2020, 26(1), pp.25-29. http://matsc.ktu.lt/index.php/MatSc/article/view/21479

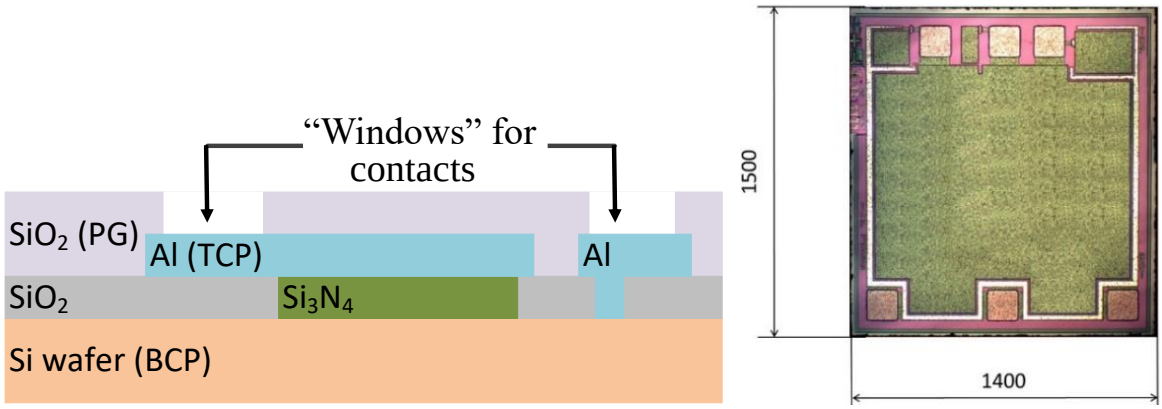

Fig. 3. Prototype 2 is a nanocapacitor with a multi-layered Si_3N_4 dielectric where a low-resistance Si wafer is used as a bottom electrode. The structure of the layers is shown on the left-hand side, the capacitor topology is shown on the right-hand side. The area of one capacitor is 2.1 mm^2. The parameters of the Si_3N_4 dielectric are shown in Table 1.

Table 2 compares the parameters of the developed prototypes with publicly available data about their modern analogues (*state-of-the-art*).

Table 2

Comparison between the developed technology prototypes and the latest publicly available analogues (*state-of-the-art*)

Parameter			Prototype 1 (uses Poly-Si electrode)		Prototype 2 (uses low-resistance Si wafer)	
			The thickness of Si_3N_4 multilayer, nm			
			40	60	40	60
Dielectric strength of the nanocapacitor dielectric layer [2], MV/cm	Developed in the project		$0.45 *10^1$	$0.47 *10^1$	$0.50 *10^1$	$0.45 *10^1$
	The modern level of development [3, 4]		$1*10^1$			
C, pF/mm^2	Developed in the project	at 10 kHz	1700	1300	2200	2200
		at 1 MHz	1700	1300	2200	2200
	The modern level of development [5]		480			
Density of leakage current I_{LEAK} in DC mode [6], A/m^2	Developed in the project		$<1,7*10^{-5}$	$<1,7*10^{-5}$	$<1,7*10^{-5}$	$<1,7*10^{-5}$
	The modern level of development [5]		$5*10^{-2}$	$1*10^{-3}$	$5*10^{-2}$	$1*10^{-3}$

[2] The ratio: (Breakdown voltage) / (thickness of the multi-layered Si_3N_4 dielectric).
[3] https://en.wikipedia.org/wiki/Silicon_nitride, viewed 26.02.2020.
[4] Yota, J. (2011). Effects of deposition method of PECVD silicon nitride as MIM capacitor dielectric for GaAs HBT technology. *ECS Transactions*, *35*(4), 229
[5] S. T. Patton, A. J. Frasca, J. W. Talnagi, D. J. Hyman, B.S. Phillips, J.G. Jones, R. A. Vaia, A. A. Voevodin. (2013). Effect of space radiation on the leakage current of MEMS insulators. *IEEE transactions on nuclear science*, *60*(4), 3074-3083.
[6] An operating voltage of 5 V and 10 V, respectively, was used to determine the parameter for 40 nm and 60 nm thick dielectric.

Parameter		Prototype 1 (uses Poly-Si electrode)		Prototype 2 (uses low-resistance Si wafer)	
		The thickness of Si_3N_4 multilayer, nm			
		40	60	40	60
Resistance to ionizing radiation					
Leakage current in DC mode, I_{LEAK}	Developed in the project	No impact	No impact	No impact	No impact
	The modern level of development [5]	No impact	No impact	No impact	No impact

The cells highlighted in yellow show parameters that are significantly superior to their modern counterparts. The parameters highlighted in grey are at the same level as their modern counterparts. In general, the comparison shows that the parameters of nanocapacitors developed in the project exceed or are at the same level as their modern counterparts.

Dissemination of the project results in scientific publications and at conferences

Five scientific articles were published in journals or conference proceedings indexed by the SCOPUS database:

1. M. Romanova, L. Avotina, M. Andrulevicius, Yu. Dekhtyar, G. Enichek, G. Kizane, M. Novotný, E. Pajuste, P. Pokorný, T. Yager, A. Zaslavski. Radiation resistance of nanolayered silicon nitride capacitors. *Nuclear Instruments and Methods in Physics Research Section B: Beam Interactions with Materials and Atoms*, 2020, 471, pp.17-23. https://doi.org/10.1016/j.nimb.2020.03.010
2. Dekhtyar, Yu., Enichek, G., Romanova, M., Schmidt, B., Vilken, A., Yager, T., Zaslavski, A. Charge Trap Analysis of nanolayer Si_3N_4 and SiO_2 by electron irradiation assisted photoelectron emission. *Physica B: Physics of Condensed Matter*, 2020, 586, 412123. https://doi.org/10.1016/j.physb.2020.412123
3. Avotina, L., Pajuste, E., Romanova, M., Enichek, G., Zaslavskis, A., Kinerte, V., Avotins, J., Dekhtyar, Yu., Kizane, G. Surface morphology of single and multilayer silicon nitride dielectric nano-coatings. *Materials Science (Medžiagotyra)*, 2020, 26(1), pp.25-29. http://matsc.ktu.lt/index.php/MatSc/article/view/21479
4. Dekhtyar, Yu., Avotiņa, L., Enichek, G., Romanova, M., Schmidt, B., Shulzinger, E., Sorokins, H., Vilken, A., Zaslavskis, A. Interface of Silicon Nitride Nanolayers with Oxygen Deficiency. *2018 16th Biennial Baltic Electronics Conference*, Estonia, Tallinn, 8-10 October, 2018. Tallinn University of Technology: 2018, pp.1-4. https://ieeexplore.ieee.org/document/8600964
5. Avotiņa, L., Pajuste, E., Romanova, M., Zaslavskis, A., Enichek, G., Kinerte, V., Zariņš, A., Lescinskis, B., Dekhtyar, Yu., Kizane, G. FTIR Analysis of Electron Irradiated Single and Multilayer Si_3N_4 Coatings. *Key Engineering Materials*, 2018, 788, pp.96-101. www.scientific.net/KEM.788.96

The results of the project were discussed at international scientific conferences:

A) *Presentations at conferences with publications in conference proceedings or abstract book:*

1. Avotina, L., Dekhtyar, Yu., Jenichek, G., Kizane, G., Pajuste, E., Romanova, M., Yager, T., Zaslavskis, A. Radiation stability of multilayer silicon nitride nanocapacitors. *20th International Conference on Radiation Effects in Insulators: Book of Abstracts*, Kazakhstan, Nur-Sultan, 19-23 August 2019.
2. Avotina, L., Romanova, M., Pajuste, E., Enichek, G., Zaslavskis, A., Dekhtyar, Yu., Kizane, G. Electrical properties of single and multilayer silicon nitride dielectric for applications in nanocapacitors. *21st International Conference-School "Advanced Materials and Technologies 2019": Book of Abstracts*, Lithuania, Palanga, 19-23 August 2019.
3. Andrulevičius, M., Avotiņa, L., Dekhtyar, Yu., Enichek, G., Romanova, M., Shulzinger, E., Sorokins, H., Tamulevičius, S., Vilken, A., Zaslavski, A. XPS, FTIR and photoelectron emission spectroscopies to analyze nanocapacitor silicon nitride nanolayered structures. *2nd International Conference on Nanomaterials Science and Mechanical Engineering: Book of Abstracts*, Portugal, Aveiro, 9-12 July 2019.
4. Yu. Dekhtyar, L. Avotiņa, G. Enichek, M. Romanova, B. Schmidt, E. Shulzinger, H. Sorokins, A. Viļķens, A. Zaslavskis. Interface of Silicon Nitride Nanolayers with Oxygen Deficiency. *2018 16th Biennial Baltic Electronics Conference*, Estonia, Tallinn, 8-10 October 2018. https://ieeexplore.ieee.org/document/8600964
5. L. Avotina, E. Pajuste, M. Romanova, A. Zaslavskis, G. Enichek, V. Kinerte, Yu. Dekhtyar, G. Kizane. Modifications of Silicon Nitride Bonds under Action of Accelerated Electrons. *RACIRI 2018 Summer School*, Germany, Rügen, 25 Aug-1 Sep. 2018.
6. E. Pajuste, M. Romanova, L. Avotina, G. Enichek, A. Zaslavskis, V. Kinerte, Yu. Dekhtyar, G. Kizane. Surface Morphology of Single and Multilayered Silicon Nitride Dielectric Nanocoatings. *20th International Conference-School "Advanced Materials and Technologies"*, Lithuania, Palanga, 27-31 August 2018
7. L. Avotina, E. Pajuste, M. Romanova, A. Zaslavskis, V. Kinerte, B. Lescinskis, Yu. Dekhtyar, G. Kizane. FT-IR Analysis of Electron Irradiated Single and Multilayer Si3N4 Coatings. *8th International Conference on Silicate Materials "BaltSilica 2018"*, Latvia, Riga, 30 May-1 Jun. 2018. https://www.scientific.net/KEM.788.96
8. L. Avotina, Yu. Dekhtyar, M. Romanova, E. Shulzinger, B. Schmidt, A. Viļķens, A. Zaslavski, G. Enichek. Silicon Nitride Multi Nanolayer System Fabricated in One Reactor. *6th International Conference "Telecommunications, Electronics and Informatics (ICTEI 2018)"*, Moldova, Chisinau, 24-27 May 2018.
9. M. Romanova, L. Avotiņa, R. Zariņš, A. Zariņš, J. Bitenieks, A. Vilimans, A. Zaslavskis, G. Kizane, Yu. Dekhtyar. Electrical properties of single-layer and multilayer Si_3N_4 dielectric on Si substrate. *3rd International Conference "Innovative Materials, Structures and Technologies" (IMST2017)*, 27-29 September 2017, Riga, Latvia.
10. L. Avotina, R. Zarins, E. Pajuste, M. Romanova, J. Bitenieks, J. Zicāns, A. Zaslavskis, Yu. Dekhtyar, G. Kizane. Influence of ionizing radiation on the Si_3N_4 coatings on Si substrate. *19th International Conference-School "Advanced Materials and Technologies 2017"*, 27-31 August 2017, Palanga, Lithuania.
11. L. Avotina, R. Zarins, M. Romanova, E. Pajuste, A. Zaslavskis, Yu. Dekhtyar, G. Kizane. Characterisation of silicon nitride coatings irradiated with accelerated electrons and bremsstrahlung radiation. *International Conference "Functional Materials and Nanotechnologies 2017" (FMNT-2017)*, 24-27 April 2017, Tartu, Estonia.

B) Oral presentations at conferences without publication:

12. L. Avotiņa, E. Pajuste, M. Romanova, A. Zaslavskis, Yu. Dekhtyar, G. Kizane. FTIR studies of radiation stability of multilayered silicon nitride thin films for nanocapacitors. *78th International Scientific Conference of the University of Latvia*, Riga, Latvia, February 21, 2020.
13. T. Yager, A. Viļķens, E. Shulzinger, Yu. Dekhtyar, G. Jeņičeks, A. Zaslavskis. Investigation of electrical defects of dielectric layers of Si_3N_4. *60th International Scientific Conference of Riga Technical University*, Riga, Latvia, October 17, 2019.
14. E. Pajuste, M. Romanova, L. Avotina, A. Zaslavskis, G. Enichek, G. Kizane, Yu. Dekhtyar. Influence of fabrication parameters on morphology of Si_3N_4 dielectric of nanocapacitor. *77th International Scientific Conference of the University of Latvia*, Riga, Latvia, February 1, 2019.
15. T. Yager, M. Romanova, Yu. Dekhtyar, A. Zaslavskis, G. Enichek, G. Kizane. Influence of manufacturing technology and ionizing radiation on electron emission properties of Si_3N_4 dielectric nanolayers. *59th International Scientific Conference of Riga Technical University*, October 11, 2018, Riga, Latvia
16. L. Avotiņa, E. Pajuste, M. Romanova, A. Zaslavskis, J. Dehtjars, G. Kizane. Characterization of chemical bonds in nanolayers of silicon nitride with FT-IR. *76th International Scientific Conference of the University of Latvia*, Riga, Latvia, February 2, 2018.
17. M. Romanova, Yu. Dekhtyar, A. Vilimans, A. Zaslavskis, G. Kizane. Study of electrical defects in Si_3N_4 dielectric layer. *58th International Scientific Conference of Riga Technical University*, October 13, 2017, Riga, Latvia.

Project photo-galleries online

- The seminar "Nanocapacitors in Latvia" organized for business companies on February 21, 2020:
  https://www.facebook.com/biedribaLETERA/posts/204933940884315
  https://www.letera.lv/letera-biedri-iepazistas-ar-inovativu-nanokondensatoru-razosanas-tehnologiju

- The photo-gallery "We aim for the global nanocapacitor market!":
  https://www.facebook.com/pg/rigastehniskauniversitate/photos/?tab=album&album_id=3643198279053551

- Information for media on a website of Riga Technical University:
  https://www.rtu.lv/lv/universitate/masu-medijiem/zinas/atvert/rada-tehnologiju-kas-var-palidzet-latvijas-uznemumiem-ieklut-pasaules-nanokondensatoru-tirgu

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