

IC Package

| release_version | Description |
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| ASSURA 4.1 | Assura(TM) Design Rule Checker |
| ASSURA 4.1 | Assura(TM) Layout Vs. Schematic Verifier |
| ASSURA 4.1 | Assura(TM) Multiprocessor Option |
| CONFRML14.1 | CCD Multi-Constraint Check Option |
| CONFRML14.1 | Encounter (R) Conformal Constraint Designer - XL |
| CONFRML14.1 | Encounter Conformal Low Power - GXL |
| CONFRML14.1 | Encounter Conformal ECO Designer - GXL |
| CTOS 14.1 | C-to-Silicon Compiler - L |
| EDI 14.1 | Encounter Digital Implementation System XL |
| EDI 14.1 | Encounter CPU Accelerator Option |
| EDI 14.1 | Encounter Mixed Signal GXL Option |
| EDI 14.1 | Encounter Giga Scale GXL Option |
| EDI 14.1 | Encounter Universal 20 GXL Option |
| EDI 14.1 | Encounter Clock Concurrent Optimization |
| EDI 14.1 | Encounter Advanced Node GXL Option |
| EDI 14.1 | Encounter Low Power GXL Option |
| ET 14.1 | Encounter True Time ATPG Advanced |
| ET 14.1 | Option to RC - DFT Architect Advanced |
| ET 14.1 | Encounter Test LBIST Option |
| ET 14.1 | Encounter Test Advanced MBIST Option |
| ET 14.1 | Encounter Diagnostics Basic |
| ETS 13.1 | Encounter Library Characterizer - GXL |
| ETS 13.1 | Encounter Power System XL |
| ETS 13.1 | EPS Advanced Analysis GXL Option |
| ETS 13.1 | Encounter Timing System-XL |
| ETS 13.1 | ETS Advanced Analysis GXL Option |
| EXT 14.1 | Cadence QRC Advanced Modeling20 GXL Option |
| EXT 14.1 | Cadence QRC Extraction - XL |
| EXT 14.1 | Cadence QRC Advanced Modeling GXL Option |
| EXT 14.1 | Cadence QRC Advanced Analysis GXL Option |
| EXT 14.1 | Cadence QRCX Display Technology Option |

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| IC 6.1.6 | Virtuoso(R) Layout Suite - GXL |
| IC 6.1.6 | Virtuoso(R) Analog Design Environment - GXL |
| IC 6.1.6 | Virtuoso Implementation Aware Design Option |
| IC 6.1.6 | Virtuoso(R) Power System XL |
| IC 6.1.6 | Virtuoso EAD Advanced Electrical Analysis |
| IC 6.1.6 | Virtuoso Layout Suite EAD |
| IC 6.1.6 | Cadence(R) SKILL Development Environment |
| IC 6.1.6 | Virtuoso(R) Layout Suite - GXL |
| IC 6.1.6 | Virtuoso(R) EDIF 200 Reader |
| IC 6.1.6 | Virtuoso(R) Layout Suite - GXL |
| IC 6.1.6 | Virtuoso(R) Schematic Editor XL |
| IC 6.1.6 | Virtuoso(R) Visualization & Analysis XL |
| IC 6.1.6 | Dracula(R) Design Rule Checker |
| IC 6.1.6 | Virtuoso(R) DFM Option |
| IC 6.1.6 | Virtuoso SMG Runtime |
| IC 6.1.6 | Virtuoso Behavioral Modeling Option |
| IC 6.1.6 | Virtuoso(R) Analog Oasis Run-Time Option |
| IC 6.1.6 | Diva(R) Layout Vs. Schematic Verifier |
| IC 6.1.6 | Diva(R) Design Rule Checker |
| IC 6.1.6 | Dracula(R) Parasitic Extractor |
| IC 6.1.6 | Diva(R) Parasitic Extractor |
| IC 6.1.6 | Virtuoso(R) Schematic VHDL Interface |
| IC 6.1.6 | Virtuoso(R) Schematic Editor Verilog(R) Interface |
| IC 6.1.6 | Virtuoso(R) EDIF 200 Writer |
| IC 6.1.6 | Virtuoso(R) AMS Designer Environment |
| IC 6.1.6 | Cadence(R) Design Framework II |
| IC 6.1.6 | Virtuoso(R) Layout Migrate |
| IC 6.1.6 | Cadence(R) OASIS for RFDE |
| IC 6.1.6 | Virtuoso(R) Schematic Editor HSPICE Interface |
| IC 6.1.6 | Dracula(R) Layout Vs. Schematic Verifier |
| IC 6.1.6 | Cadence Framework Integration Runtime Option |
| IC 6.1.6 | Cadence(R) Design Framework Integrator's Toolkit |
| IC 6.1.6 | Virtuoso(R) Simulation Environment |

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| IC 6.1.6 | Virtuoso(R) Analog HSPICE Interface Option |
| IC 6.1.6 | Virtuoso(R) Layout Suite - GXL |
| IC 6.1.6 | Virtuoso EAD 3D Precision Solver |
| INCISIV 14.1 | Incisive Advanced Option |
| INCISIV 14.1 | Incisive Software Extensions |
| INCISIV 14.1 | Cadence(R) Export Model Packager |
| INCISIV 14.1 | Incisive Formal Verifier |
| INCISIV 14.1 | Incisive Low-Power Simulation Option |
| INCISIV 14.1 | AMS Designer with Flexible Analog Simulation |
| INCISIV 14.1 | Virtuoso AMS Designer Verification Option |
| INCISIV 14.1 | Digital Mixed Signal Option to IES |
| INCISIV 14.1 | Incisive Enterprise Simulator - XL |
| INCISIV 14.1 | Incisive Enterprise Verifier - XL |
| INCISIV 14.1 | Verifault(R)-XL simulator |
| INCISIV 14.1 | Incisive Enterprise Manager |
| LIBERATE 13.1 | Virtuoso Liberate LV Client |
| LIBERATE 13.1 | Virtuoso Liberate LV Server |
| LIBERATE 13.1 | Virtuoso Liberate Client |
| LIBERATE 13.1 | Virtuoso Variety Client |
| LIBERATE 13.1 | Virtuoso Variety MX Server |
| LIBERATE 13.1 | Virtuoso Liberate Server |
| LIBERATE 13.1 | Virtuoso Variety Server |
| LIBERATE 13.1 | Virtuoso Liberate AMS Server |
| LIBERATE 13.1 | Virtuoso Liberate MX Client |
| LIBERATE 13.1 | Virtuoso Variety MX Client |
| LIBERATE 13.1 | Virtuoso Liberate MX Server |
| LIBERATE 13.1 | Virtuoso Liberate AMS Client |

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| MMSIM 13.1 | Spectre Extensive Partitioned Simulator |
| MMSIM 13.1 | Virtuoso(R) Spectre Model Interface Option |
| MMSIM 13.1 | Virtuoso(R) RelXpert |
| MMSIM 13.1 | Virtuoso Multi-mode Simulation with AP Simulator |
| MMSIM 13.1 | Virtuoso Multi-mode Simulation with AP Simulator |
| MMSIM 13.1 | Virtuoso Multi-mode Simulation CPU Accelerator option |
| MVS 14.1 | Encounter DFM GXL Option |
| MVS 14.1 | Virtuoso LDE Analyzer Option |
| PVS 14.1 | Cadence(R) Physical Verification System Programmable Electrical Rules Checker |
| PVS 14.1 | Cadence Physical Verification System Advanced Metal Fill Option for PVS DRC XL (96210) |
| PVS 14.1 | PVS Design Analysis Option |
| PVS 14.1 | PVS Design Analysis Option |
| PVS 14.1 | Cadence(R) Physical Verification System Graphic LVS Debugger |
| PVS 14.1 | Cadence(R) Physical Verification System Layout vs. Schematic Checker XL |
| PVS 14.1 | Cadence(R) Physical Verification System Layout vs. Schematic Checker XL |
| PVS 14.1 | Cadence(R) Physical Verification System Design Rule Checker XL |
| PVS 14.1 | Cadence(R) Physical Verification System Design Rule Checker XL |
| PVS 14.1 | Virtuoso Integrated Physical Verification System Advanced Analysis Option for IPVS (96400) |
| PVS 14.1 | Cadence(R) Physical Verification System Advanced Device Parameter Extraction Option for PVS LVS XL (96220) |
| PVS 14.1 | Cadence(R) Physical Verification System Interactive Short Locator Option |
| PVS 14.1 | Virtuoso(R) Integrated Physical Verification System Option for Virtuoso Layout Suite (95300, 95310) |
| PVS 14.1 | Cadence(R) Physical Verification System Hierarchical DFM SignOff Option |
| PVS 14.1 | Cadence Physical Verification System Advanced Analysis Option for PVS DRC XL (96210) |
| PVS 14.1 | Cadence Physical Verification System Advanced Analysis Option for PVS DRC XL (96210) |
| PVS 14.1 | Cadence(R) Physical Verification System Constraint Validator |
| PVS 14.1 | Cadence(R) QuickView Layout and Mask Data Viewer |
| PVS 14.1 | Cadence QuickView Sign-Off Data Analysis Environment |
| RC 14.1 | Encounter RTL Compiler - XL |
| RC 14.1 | Encounter RTL Compiler CPU Accelerator Option |
| RC 14.1 | Encounter RTL Compiler Low Power Option |
| RC 14.1 | Encounter RTL Compiler Advanced Physical Option |

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| SSV 14.1 | Voltus IC Power Integrity Solution - XL (VTS-XL) |
| SSV 14.1 | Tempus Timing Signoff Solution XL |
| SSV 14.1 | Voltus IC Power Integrity Solution Advanced Analysis GXL Option (VTS-AA) |
| SSV 14.1 | Tempus Timing Signoff Solution MP |
| SSV 14.1 | Tempus Timing Signoff Solution TSO |
| SSV 14.1 | Voltus IC Power Integrity Solution - MP (VTS-MP) (Acceleration Option to Voltus IC XL (VTS200)) |
| VIPCAT 11.3 | Memory Model Portfolio |
| VIPCAT 11.3 | Memory Model for Flash PPN DDR |
| VIPCAT 11.3 | VIP for USB 3.0 & OTG |
| VIPCAT 11.3 | Memory Model for LRDIMM |
| VIPCAT 11.3 | VIP for HDMI 1.4 |
| VIPCAT 11.3 | VIP for MR-IOV |
| VIPCAT 11.3 | VIP for OCP 3.0 |
| VIPCAT 11.3 | VIP for PCI Express 3.0 |
| VIPCAT 11.3 | SOC Portfolio |
| VIPCAT 11.3 | VIP for PCI Express 1.1 & 2.0 PureSuite - Initial Release |
| VIPCAT 11.3 | VIP for SATA 6G |
| VIPCAT 11.3 | VIP for MIPI SLIMbus |
| VIPCAT 11.3 | Memory Model for Flash Toggle NAND 2 |
| VIPCAT 11.3 | Memory Model for Flash ONFi 3 |
| VIPCAT 11.3 | PureView |